What is claimed is:

1. An interconnect comprising:

a trench having a depth and a width, the depth being greater than a critical depth; and

a number of metal layers above the trench, wherein the number of metal layers is determined by the width.

2. The interconnect of claim 1, further comprising:

a number of metal stack layers including the number of metal layers above the trench, wherein the number of metal stack layers has a thickness, and the critical depth is equal to a second thickness of a second number of metal stack layers equal to one less than the number of metal stack layers.

3. The interconnect of claim 2, wherein at least one of the number of metal layers is fabricated from copper.

4. An interconnect comprising:

a trench having a width and a depth, the depth being greater than a critical depth;

a number of metal stack layers capable of defining a critical width and located above the trench; and

a number of metal layers above the trench, wherein the number of metal layers above the trench is a function of the width and the critical width.

5. The interconnect of claim 4, wherein the width is greater than the critical width.

6. The interconnect of claim 4, wherein each of the number of metal stack layers is planarized by chemical mechanical polishing.

7. An interconnect comprising:

a trench having a depth and a width; and

a number of metal layers above the trench, wherein for the depth being greater than a critical depth, the number of metal layers are capable of being increased as the width increases.

8. An interconnect comprising:

a trench having a trench depth greater than a critical depth;

a number of metal stack layers above the trench, the number of metal stack layers having a thickness; and

a number of metal layers above the trench, wherein the number of metal layers is capable of being increased as the thickness decreases.

9. The interconnect of claim 8, wherein at least one of the number of metal stack layers above the trench couples a first logic device to a second logic device.

10. An interconnect comprising:

a first memory cell;

a second memory cell;

a trench having a trench depth greater than a critical depth; and

a number of metal stack layers above the trench, wherein each of the number of metal stack layers has a sidewall thickness, the number of metal stack layers above the trench is capable of being increased as the sidewall thickness decreases, and at least one of the number of metal stack layers couples the first memory cell to the second memory cell.

11. An interconnect comprising:

a first trench having a depth greater than a critical depth and a width less than twice a first sidewall thickness;

a second trench having the depth of the first trench and a width greater than twice the first sidewall thickness and less than twice a sum of the first sidewall thickness and a second sidewall thickness;

a first metal layer above the first trench and the second trench; and

a second metal layer above the second trench.

12. The interconnect of claim 11, wherein the first metal layer above the first trench couples a first integrated circuit device to a second integrated circuit device in a memory module.

13. The interconnect of claim 11, wherein the first metal layer above the first trench couples a first integrated circuit device to a second integrated circuit device in a logic module.

14. The interconnect of claim 11, wherein the second metal layer is fabricated from Al-Cu.

15. An interconnect comprising:

a first trench having a top and a depth greater than a critical depth, and a width less than a sidewall width of a first metal;

a second trench having a depth greater than a second critical depth, and a width greater than twice the sidewall width of the first metal and less than twice a sidewall width of a second metal; and

a first and a second metal deposited on the first trench and the second trench, the second metal is planarized to the top of the first trench.

16. The interconnect of claim 15, wherein the second metal comprises Al.

17. The interconnect of claim 15, wherein the second metal is planarized by chemical mechanical polishing.

18. A method for forming an interconnect comprising:

selecting an insulative surface;

selecting a number of metallization stack layers having a critical thickness;

etching a trench on the insulative surface, the trench having a depth greater than the critical thickness and a width less than a sidewall thickness of a first metallization stack, and the trench coupling a first memory cell to a second memory cell;

etching a second trench on the insulative surface, the second trench having a depth greater than the critical thickness and a width greater than the sidewall thickness and less than a second sidewall thickness of a second metallization stack;

depositing the first metal layer;

depositing the second metal layer; and

planarizing the insulative surface.

19. The method of claim 18, wherein depositing a first metal comprises depositing copper.

20. The method of claim 18, wherein planarizing the insulative surface comprises planarizing by chemical mechanical polishing.

21. A method for dimensioning a trench comprising:

selecting a number of layers, the number of layers having a sidewall thickness;

selecting a second number of layers having a second sidewall thickness, wherein the second number of layers has one less metal layer than the number of layers;

identifying a critical depth; and

dimensioning the trench to have a depth greater than the critical depth and a width less than the sidewall thickness but greater than the second sidewall thickness.

22. The method of claim 21, wherein identifying a critical depth comprises:

calculating a total bottom thickness for one less layer than the number of layers, the total bottom thickness being the critical depth.

23. An interconnect comprising:

a trench having a width and a metal layer; and

a second trench having a depth greater than a critical depth and a second width greater than the width, the second trench having a plurality of metal layers and at least one of the plurality of metal layers is coupled to the metal layer.

24. The interconnect of claim 23, further comprising a wire bond coupling a conductive material to at least one of the plurality of metal layers.

25. The interconnect of claim 24, wherein at least one of the plurality of metal layers is aluminum.

26. An interconnect comprising:

a trench having a depth greater than a critical depth and a copper layer; and

a second trench wider than the trench, and the second trench having a plurality of metal layers, wherein at least one of the plurality of layers is an aluminum layer, and at least one of the plurality of metal layers is coupled to the copper layer.

27. The interconnect of claim 26, wherein the aluminum layer is an aluminum alloy layer.

28. The interconnect of claim 26, wherein at least one of the plurality of metal layers is a copper layer.

29. The interconnect of claim 26, wherein the aluminum layer is wire-bonded to a conductive material.

30. The interconnect of claim 29, wherein the conductive material is gold.

31. An interconnect comprising:

a trench having a critical depth, a width, a barrier layer, and a metal layer over the barrier layer; and

a second trench having a second width greater than the width and the second trench having a barrier layer, a copper layer over the barrier layer, a titanium layer over the copper layer, a titanium nitride layer over the titanium layer, and an aluminum alloy layer over the titanium nitride layer.

32. The interconnect of claim 31, wherein the barrier layer comprises TiN.

33. The interconnect of claim 31, wherein the aluminum alloy layer is planarized by chemical mechanical polishing.

34. An interconnect comprising:

a trench, a barrier layer, and a metal layer over the barrier layer; and

a second trench, a barrier layer, a copper layer over the barrier layer, a tantalum layer over the copper layer, a tantalum nitride layer over the tantalum layer, and an aluminum alloy layer over the tantalum nitride layer.

35. The interconnect of claim 34, wherein the barrier layer comprises Ti/TiN.

36. A conductive structure comprising:

a trench having a barrier layer and a metal layer over the barrier layer; and

a second trench wider than the trench and the second trench having a barrier layer, a copper layer over the barrier layer, a tantalum layer over the copper layer, a tantalum nitride layer over the tantalum layer, and an aluminum alloy layer over the tantalum nitride layer.

37. The conductive structure of claim 36, wherein the barrier layer comprises TaN.

38. The conductive structure of claim 36, wherein the aluminum alloy layer comprises Al-Si-Cu.

39. The conductive structure of claim 36, wherein the copper layer is planarized by chemical mechanical polishing.

40. A conductive structure comprising:

a trench having a barrier layer and a metal layer over the barrier layer; and

a second trench having a depth greater than a critical depth, a barrier layer, a copper layer over the barrier layer, a tantalum layer over the copper layer, and an aluminum alloy layer over the tantalum layer.

41. The conductive structure of claim 40, wherein the metal layer is copper.

42. The conductive structure of claim 40, wherein the aluminum alloy is aluminum-copper.

43. The conductive structure of claim 40, wherein the barrier layer is Ta/TaN.

44. An interconnect comprising:

a trench having a width and a barrier layer and a metal layer over the barrier layer; and

a second trench having a barrier layer, a copper layer over the barrier layer, a tantalum nitride layer over the copper layer, and an aluminum alloy layer over the tantalum nitride layer.

45. The interconnect of claim 44, wherein the second trench has a second width greater than the width.

46. The interconnect of claim 45, wherein the barrier layer is a refractory metal nitride.

47. The interconnect of claim 46, wherein the tantalum nitride layer is planarized by chemical mechanical polishing.

48. An interconnect comprising:

a trench having a depth less than a critical depth and a width less than a critical width and a metal layer; and

a second trench having a depth greater than a critical depth;

a plurality of metal layers above the second trench, at least one of the plurality of metal layers is coupled to the metal layer, wherein at least one of the plurality of metal layers is capable of forming a highly reliable eutectic bond to a conductive material.

49. The interconnect of claim 48, wherein the metal layer is copper.

50. The interconnect of claim 49, wherein at least of the plurality of metal layers is aluminum.

51. The interconnect of claim 48, wherein at least one of the plurality of metal layers is an aluminum alloy.

52. An interconnect comprising:

a trench having a metal layer and a depth greater than a critical depth; and

a second trench having a plurality of metal layers, at least one of the plurality of metal layers is coupled to the metal layer, wherein only one of the plurality of metal layers is capable of forming a highly reliable eutectic bond to a gold wire.

53. The interconnect of claim 52, wherein the second trench has a depth greater than the critical depth.

54. A conductive structure comprising:

a trench having a width, a depth, and a metal layer; and

a second trench having a width, a depth and a plurality of metal layers, the width of the second trench is greater than the width of the trench, and at least one of the plurality of the metal layers is capable of being electrically coupled to the metal layer.

55. The conductive structure of claim 54, wherein at least one of the plurality of the metal layers is wire-bonded to a highly conductive wire.

56. The conductive structure of claim 55, wherein the highly conductive wire is a gold alloy.

57. A conductive structure comprising:

a narrow trench having a metal layer and a depth greater than a critical depth; and

a wide trench having a plurality of metal layers and a second depth equal to the depth, wherein at least one of the plurality of metal layers is coupled to the metal layer.

58. An interconnect comprising:

a trench having a width less than a critical width, a depth and a metal layer; and

a wide depression having a second width greater than the critical width, a second depth equal to the depth, and a plurality of metal layers, wherein at least one of the plurality of metal layers is coupled to the metal layer.

59. The interconnect of claim 58, wherein the depth is greater than a critical depth.

60. The interconnect of claim 59, wherein at least one of the plurality of metal layers is eutectically wire-bonded to a gold wire.

61. A method of forming a conductive structure comprising:

etching a trench having a depth greater than a critical depth in a substrate having a surface;

under filling the trench with a first conductive material;

overfilling the trench with a second conductive material suitable for high reliability wire-bonding; and

polishing the substrate until the first conductive material and the second conductive material are removed from the surface of the substrate.

62. The method of claim 61, wherein polishing the substrate until the first conductive material and the second conductive material are removed from the surface of the substrate comprises:

applying chemical mechanical polishing to remove the first conductive material and the second conductive material from the surface of the substrate.

63. A method of forming a conductive structure comprising:

etching a fine line trench to a depth greater than a critical depth in a substrate having a surface;

etching a wide line trench to the depth in the substrate such that the wide line trench intersects the fine line trench;

filling the fine line trench with a first conductive material;

under filling the wide line trench with the first conductive material;

filling the wide line trench with a second conductive material suitable for high reliability wire-bonding; and

polishing the substrate until the first conductive material and the second conductive material are removed from the surface of the substrate.

64. The method of claim 63, wherein filling the fine line trench with a first conductive material comprises:

overfilling the fine line trench with a first conductive material.

65. The method of claim 63, wherein filling the wide line trench with a second conductive material suitable for high reliability wire-bonding comprises:

under filling the wide line trench with a second conductive material suitable for high reliability wire-bonding

66. A method of forming a conductive structure comprising:

etching a wide line trench having a depth greater than a critical depth in the substrate;

depositing a seed layer above the surface of the substrate;

depositing a layer of conductive material above the seed layer such that the conductive material under fills the wide line trench;

depositing a barrier layer above the layer of conductive material;

depositing a second layer of conductive material above the barrier layer, the second layer of conductive material is capable of reliably wire bonding to a gold wire; and

removing the seed layer, the layer of conductive material, the barrier layer, and the second layer of conductive material from the surface of the substrate.

67. The method of claim 66, wherein depositing a layer of conductive material above the seed layer such that the conductive material under fills the wide line trench comprises:

electroplating a layer of copper above the seed layer such that the copper under fills the wide line trench.

68. The method of claim 66, wherein depositing a second layer of conductive material above the barrier layer, the second layer of conductive material is capable of reliably wire bonding to a gold wire comprises:

depositing a layer of aluminum above the barrier layer, the aluminum layer is capable of reliably wire bonding to a gold wire.

69. A computer system comprising:

a processor;

a device coupled to the processor; and

a interconnect coupled to the device, the interconnect comprising:

a trench having a depth greater than a critical depth and a metal layer; and

a bond pad trench having a bond pad depth equal to the depth and a plurality of metal layers coupled to the metal layer.

70. The computer system of claim 69, further comprising:

a conductive wire eutectically bonded to at least one of the plurality of metal layers.

71. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a trench having a depth greater than a critical depth, a barrier layer, and a copper layer above the barrier layer;

a bond pad trench having a barrier layer, the bond pad trench having a copper layer above the barrier layer, and the bond pad trench having a titanium layer above the copper layer, and an aluminum-copper layer above the titanium layer.

72. A computer system comprising:

a processor;

a device coupled to the processor; and

an interconnect coupled to the device, the interconnect comprising:

a fine line having a conductive layer; and

a wide line having a number of conductive layers, and at least one of the number of conductive layers of the wide line being coupled to the fine line.

73. The computer system of claim 72, wherein the wide line is capable of being reliably wire bonded to a conductive gold wire.

74. A computer system comprising:

a processor;

a device coupled to the processor; and

an interconnect coupled to the device, the interconnect comprising:

a fine line having a depth greater than a critical depth, a barrier layer and a layer of electroplated copper; and

a wide line having a wide line depth equal to the depth, a number of conductive layers, and at least one of the number of conductive layers coupled to the electroplated copper.

75. The computer system of claim 74, wherein at least one of the number of conductive layers is wire-bonded to a gold wire.

76. The computer system of claim 74, wherein a eutectic bond is used to wire-bond at least one of the number of conductive layers to a gold wire.

77. A computer system comprising:

a processor;

a device coupled to the processor; and

a conductive structure coupled to the device, the conductive structure comprising:

a fine line having a layer of electroplated copper; and

a wide line having a number of conductive layers, at least one of the number of conductive layers is capable of eutectic bonding to a gold wire, and the wide line is coupled to the fine line.

78. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a fine line having a single layer of electroplated copper having a depth greater than a critical depth; and

a wide line having a stack of conductive layers capable of eutectic bonding to a gold wire, and the wide line coupled to the fine line and the wide line having a depth greater than a critical depth.

79. A computer system comprising:

a processor;

a device coupled to the processor; and

a conductive structure coupled to the device, the conductive structure comprising:

a fine line having a depth greater than a critical depth and a single layer of electroplated copper; and

a wide line having a wide line depth equal to the depth, and a stack comprising a barrier layer, a copper layer, and an aluminum layer capable of eutectic bonding to a conductive material, and the wide line coupled to the fine line.

80. The computer system of claim 79, wherein the barrier layer comprises a refractory metal/refractory metal nitride.